

1        WHAT IS CLAIMED IS:

2            1.        An integrated circuit comprising:  
3                    a plurality of logic cells; and  
4                    a rearrangeable programmable network interconnecting said logic cells, said  
5                    programmable interconnection network having:  
6                          a plurality of programmable switches, each programmable switch having a  
7                          plurality of input terminals and a number of output terminals, signals on any input terminal  
8                          passed to any output terminal responsive to a programming of said switch,  
9                          said plurality of programmable switches arranged in a Benes network so as to  
10                  form a rearrangeable network.

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12            2.        The integrated circuit of claim 1 wherein each of said programmable switches  
13                  has two input terminals.

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15            3.        The integrated circuit of claim 1 wherein said integrated circuit comprises an  
16                  FPGA.

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18            4.        The integrated circuit of claim 1 wherein each programmable switch has a  
19                  plurality of latches responsive to clock signals for passing signals through said programmable  
20                  interconnection network in a pipelined fashion to avoid uncertainties in signal routing delays  
21                  through said programmable interconnection network.

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23            5.        The integrated circuit of claim 1 wherein predetermined ones of  
24                  programmable switches each have a plurality of latches responsive to clock signals for  
25                  passing signals through said programmable interconnection network in a pipelined fashion to  
26                  avoid uncertainties in signal routing delays through said programmable interconnection  
27                  network.